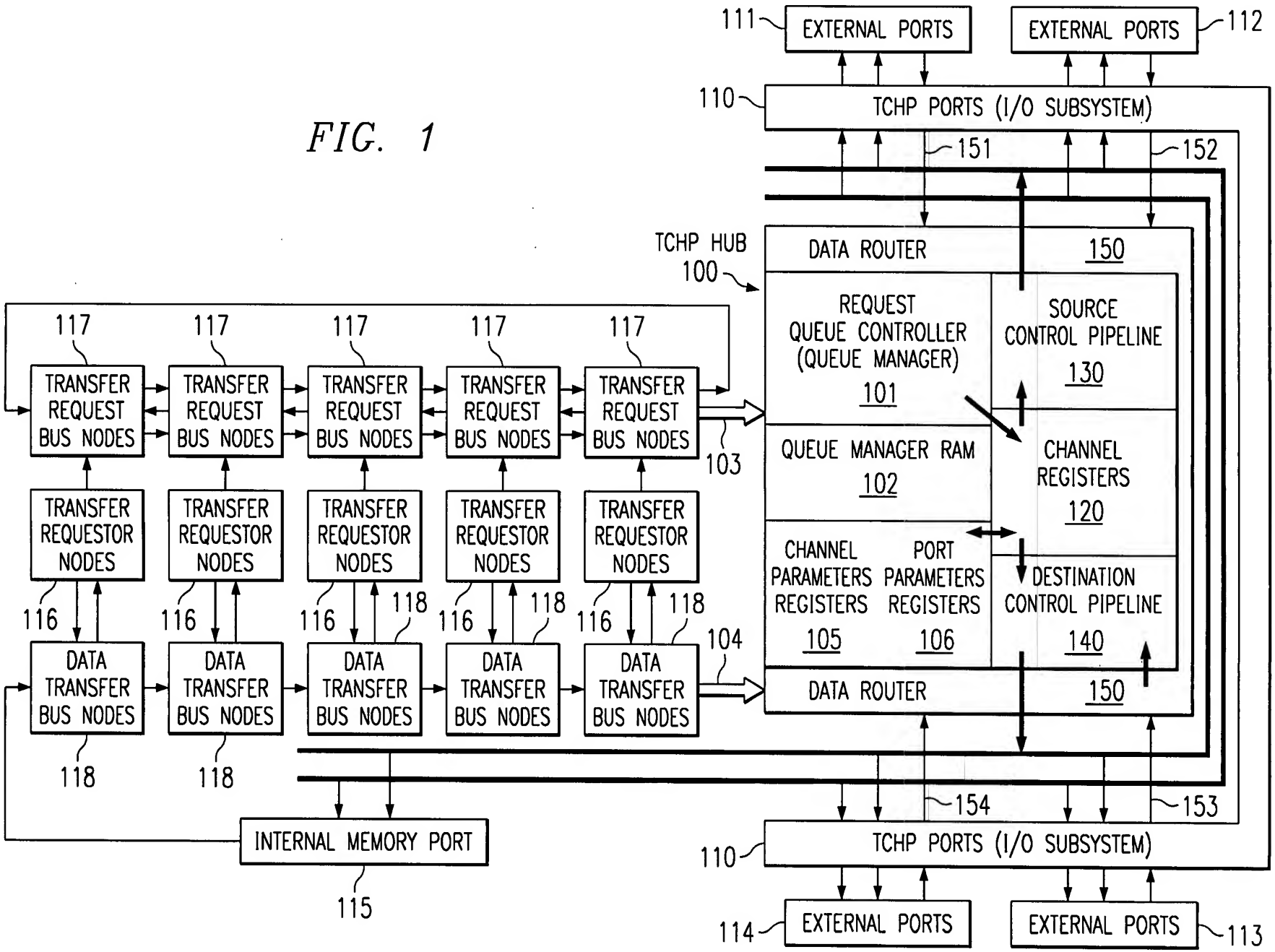
FIG. 1


111
EXTERNAL PORTS
EXTERNAL PORTS
112
110
TCHP PORTS (I/O SUBSYSTEM)
151
152
TCHP HUB
100
DATA ROUTER
150
REQUEST QUEUE CONTROLLER (QUEUE MANAGER)
101
SOURCE CONTROL PIPELINE
130
QUEUE MANAGER RAM
102
CHANNEL REGISTERS
120
CHANNEL PARAMETERS REGISTERS
105
PORT PARAMETERS REGISTERS
106
DESTINATION CONTROL PIPELINE
140
DATA ROUTER
150
117
TRANSFER REQUEST BUS NODES
103
TRANSFER REQUESTOR NODES
116
118
DATA TRANSFER BUS NODES
104
INTERNAL MEMORY PORT
115
154
153
TCHP PORTS (I/O SUBSYSTEM)
110
114
EXTERNAL PORTS
EXTERNAL PORTS
113

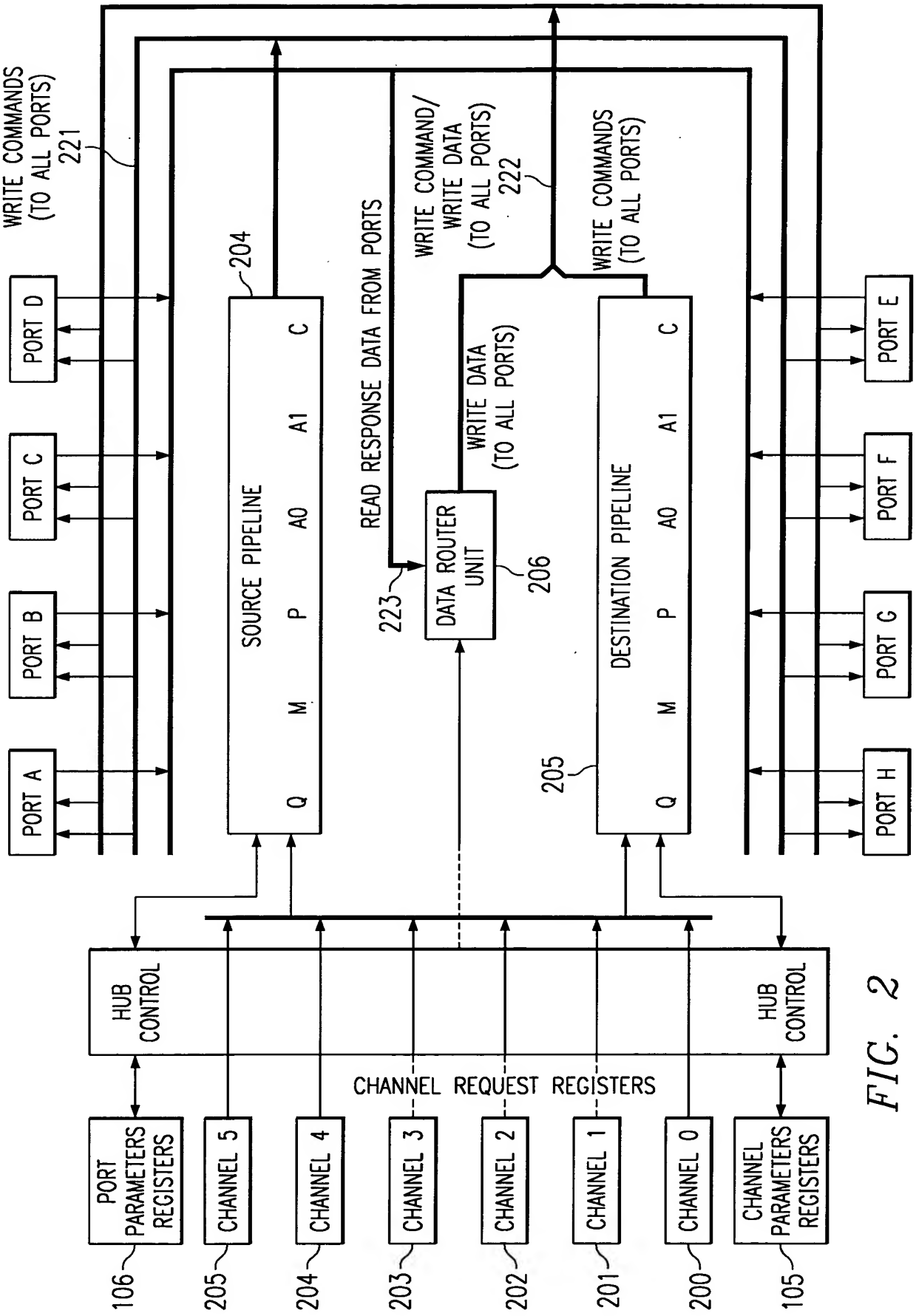
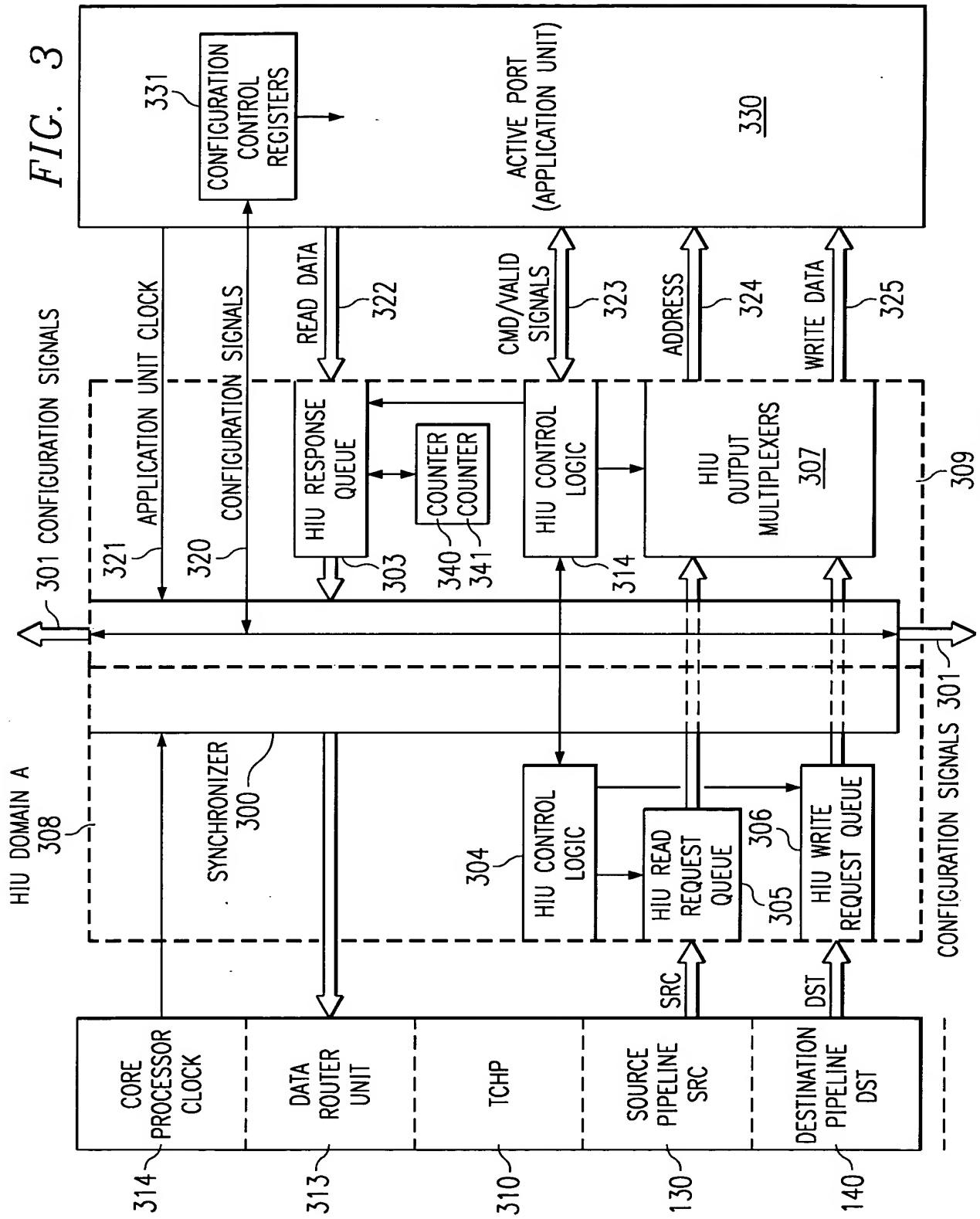

READ/PRE-WRITE COMMANDS (TO ALL PORTS)
221
WRITE COMMAND/ WRITE DATA (TO ALL PORTS)
222
WRITE COMMANDS (TO ALL PORTS)
READ RESPONSE DATA FROM PORTS
WRITE DATA (TO ALL PORTS)
PORT A
PORT B
PORT C
PORT D
PORT E
PORT F
PORT G
PORT H
SOURCE PIPELINE
Q M P A0 A1 C
204
DESTINATION PIPELINE
Q M P A0 A1 C
205
DATA ROUTER UNIT
206
223
HUB CONTROL
HUB CONTROL
CHANNEL REQUEST REGISTERS
PORT PARAMETERS REGISTERS
106
CHANNEL 5
205
CHANNEL 4
204
CHANNEL 3
203
CHANNEL 2
202
CHANNEL 1
201
CHANNEL 0
200
CHANNEL PARAMETERS REGISTERS
105

FIG. 2

FIG. 3


331
CONFIGURATION CONTROL REGISTERS
ACTIVE PORT (APPLICATION UNIT)
330
READ DATA
322
CMD/VALID SIGNALS
323
ADDRESS
324
WRITE DATA
325
301 CONFIGURATION SIGNALS
APPLICATION UNIT CLOCK
321
CONFIGURATION SIGNALS
320
HIU RESPONSE QUEUE
303
COUNTER
COUNTER
340
341
HIU CONTROL LOGIC
314
HIU OUTPUT MULTIPLEXERS
307
309
HIU DOMAIN B
HIU DOMAIN A
308
SYNCHRONIZER
300
304
HIU CONTROL LOGIC
HIU READ REQUEST QUEUE
306
305
HIU WRITE REQUEST QUEUE
CONFIGURATION SIGNALS 301
SRC
DST
CORE PROCESSOR CLOCK
DATA ROUTER UNIT
TCHP
SOURCE PIPELINE SRC
DESTINATION PIPELINE DST
314
313
310
130
140

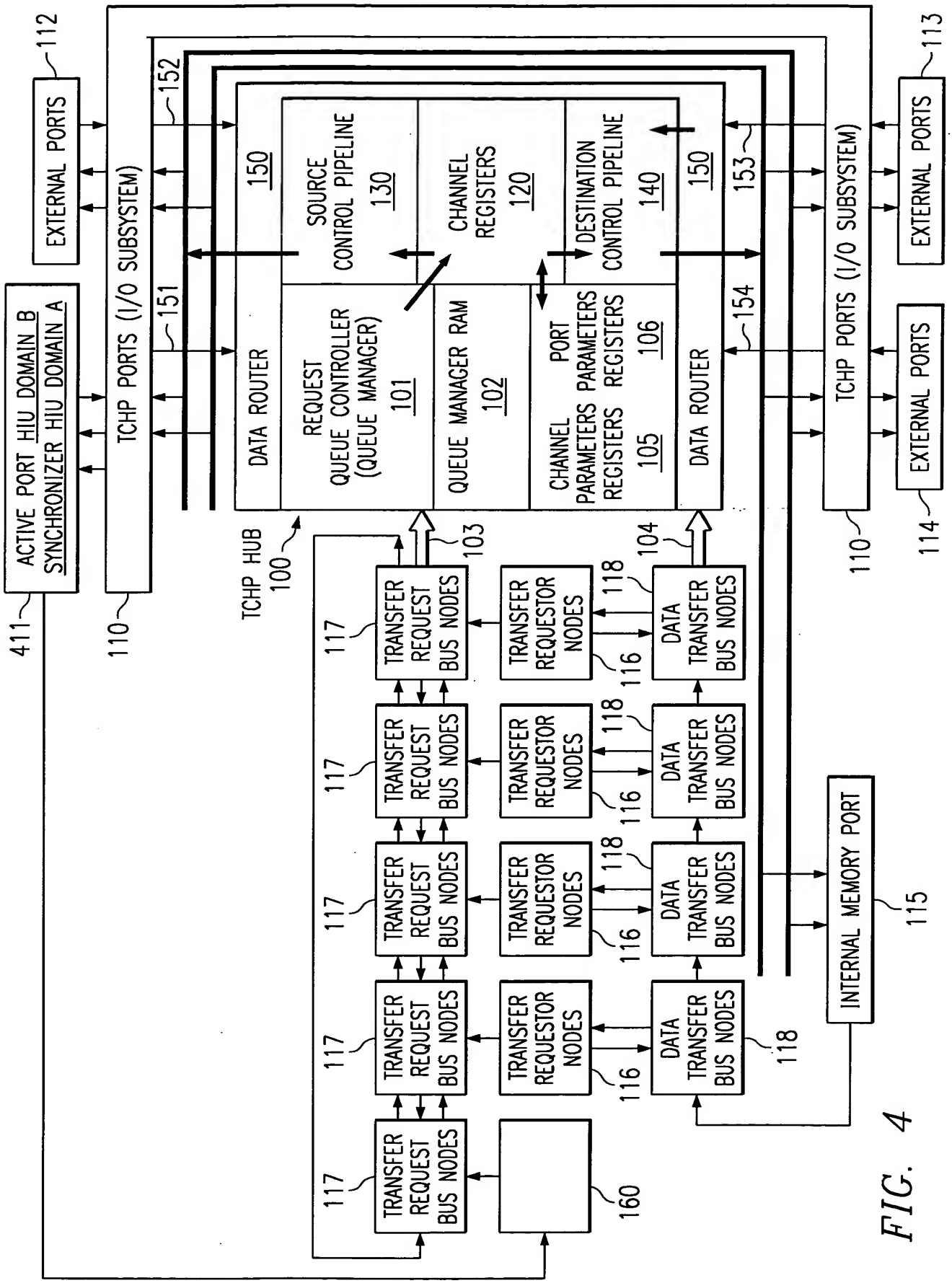

EXTERNAL PORTS
112
ACTIVE PORT HIU DOMAIN B
SYNCHRONIZER HIU DOMAIN A
411
TCHP PORTS (I/O SUBSYSTEM)
110
151
152
DATA ROUTER
150
REQUEST QUEUE CONTROLLER (QUEUE MANAGER)
101
SOURCE CONTROL PIPELINE
130
CHANNEL REGISTERS
120
DESTINATION CONTROL PIPELINE
140
QUEUE MANAGER RAM
102
CHANNEL PORT PARAMETERS REGISTERS
105
PARAMETERS REGISTERS
106
DATA ROUTER
150
153
154
TCHP HUB
100
103
104
TCHP PORTS (I/O SUBSYSTEM)
110
EXTERNAL PORTS
113
EXTERNAL PORTS
114
TRANSFER REQUEST BUS NODES
117
TRANSFER REQUESTOR NODES
116
DATA TRANSFER BUS NODES
118
INTERNAL MEMORY PORT
115
160

FIG. 4

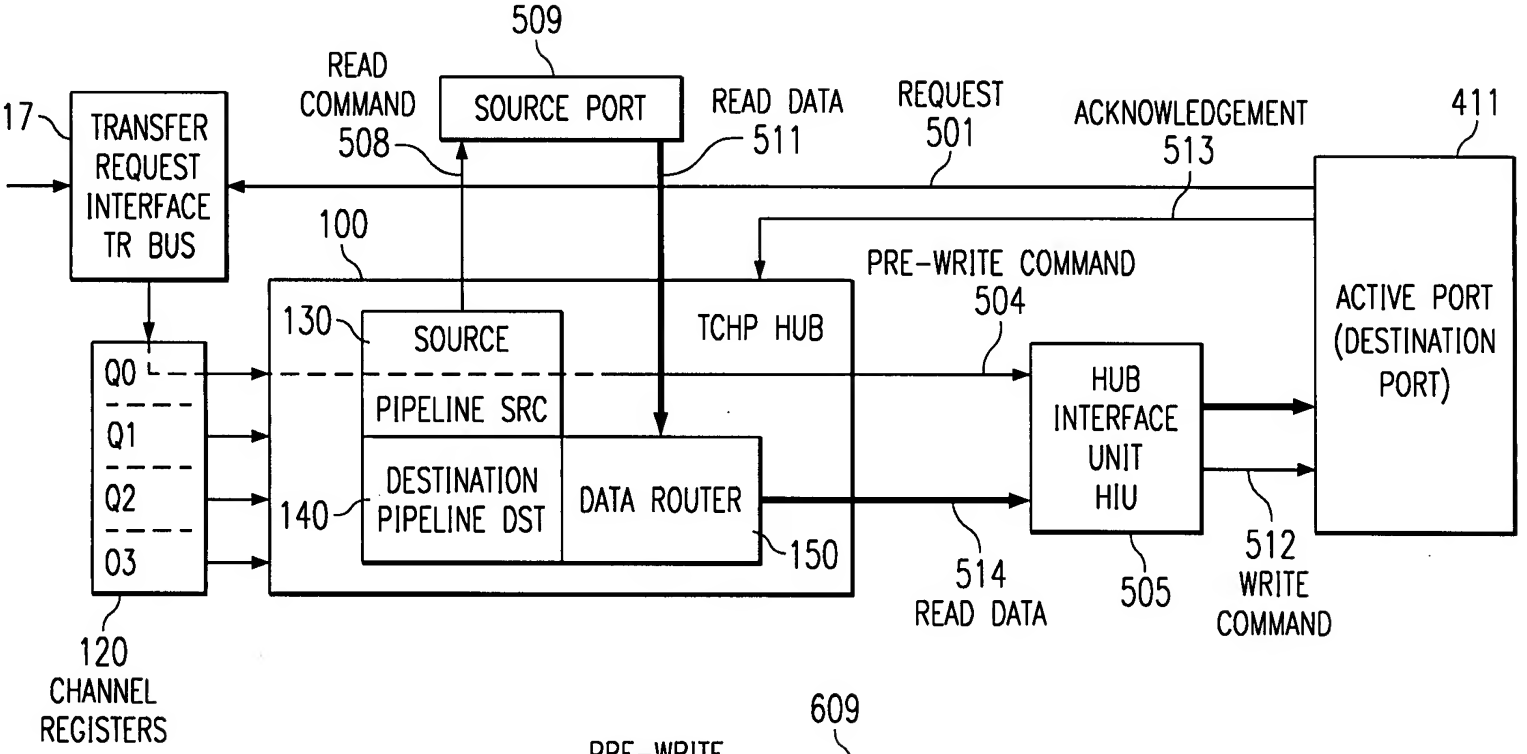

509
READ COMMAND
508
SOURCE PORT
READ DATA
511
REQUEST
501
ACKNOWLEDGEMENT
513
411
117
TRANSFER REQUEST INTERFACE TR BUS
100
PRE-WRITE COMMAND
504
130
SOURCE
TCHP HUB
ACTIVE PORT (DESTINATION PORT)
Q0
Q1
Q2
03
PIPELINE SRC
HUB INTERFACE UNIT HIU
DESTINATION PIPELINE DST
DATA ROUTER
140
150
514
READ DATA
505
512
WRITE COMMAND
120
CHANNEL REGISTERS

FIG. 5

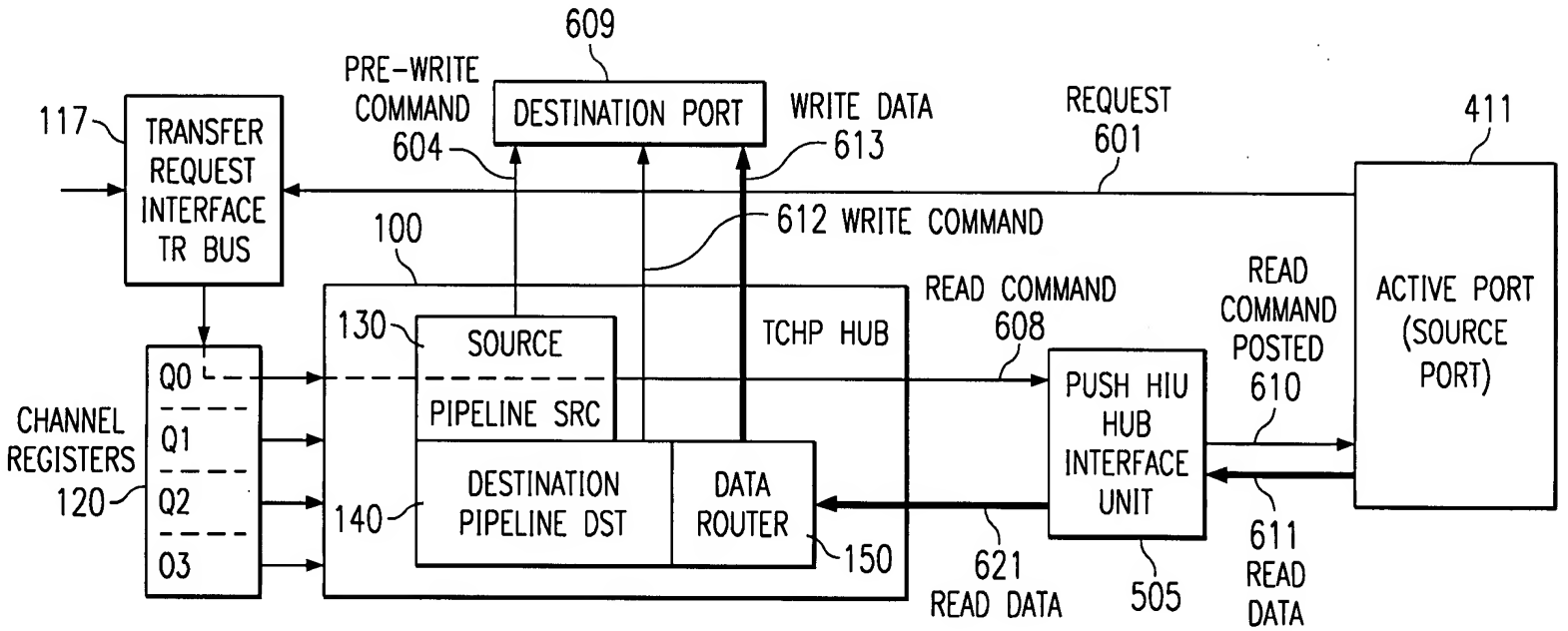

609
PRE-WRITE COMMAND
604
DESTINATION PORT
WRITE DATA
613
REQUEST
601
411
117
TRANSFER REQUEST INTERFACE TR BUS
612 WRITE COMMAND
100
READ COMMAND
608
READ COMMAND POSTED
610
ACTIVE PORT (SOURCE PORT)
130
SOURCE
TCHP HUB
Q0
Q1
Q2
03
PIPELINE SRC
PUSH HIU HUB INTERFACE UNIT
CHANNEL REGISTERS
120
DESTINATION PIPELINE DST
DATA ROUTER
140
150
621
READ DATA
505
611
READ DATA

FIG. 6

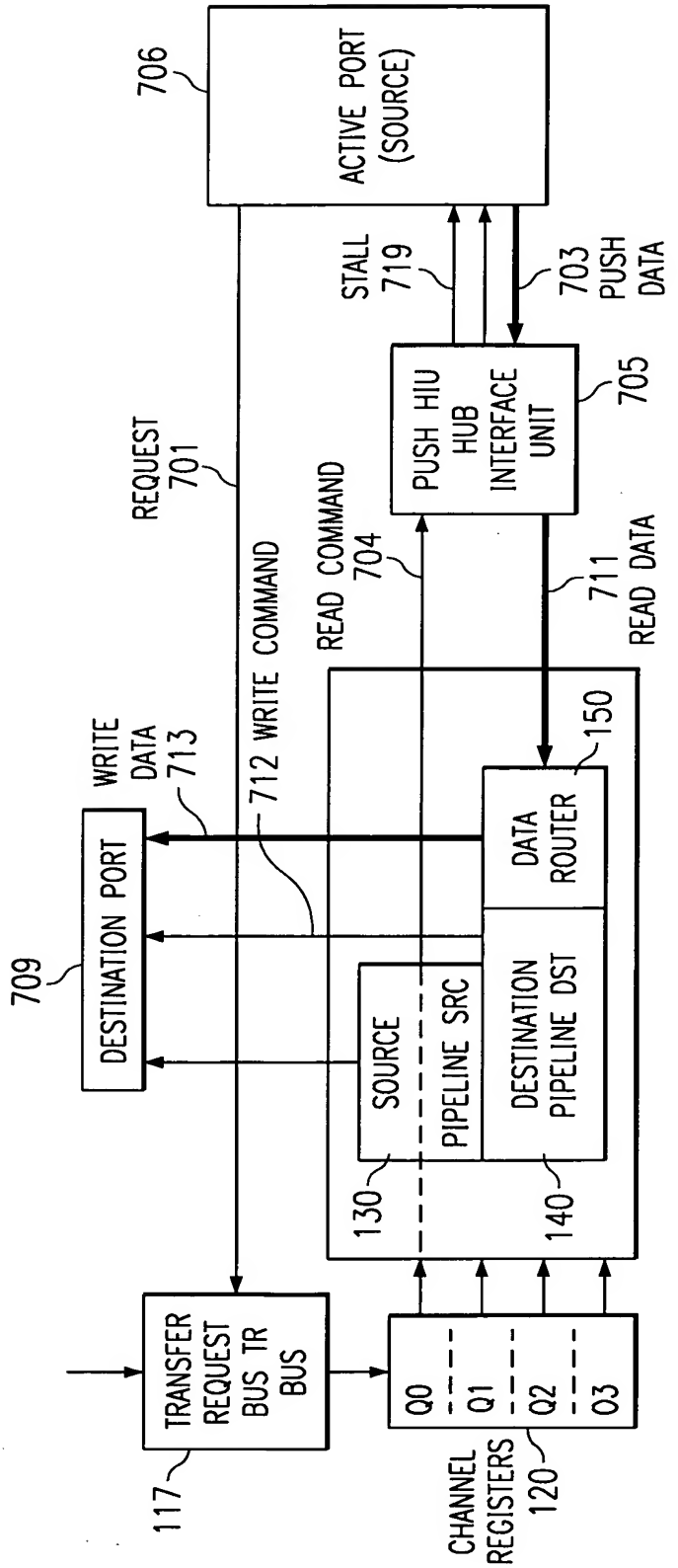

706
ACTIVE PORT (SOURCE)
STALL 719
703 PUSH DATA
PUSH HIU HUB INTERFACE UNIT
705
REQUEST 701
READ COMMAND 704
711 READ DATA
712 WRITE COMMAND
WRITE DATA 713
150
DATA ROUTER
709
DESTINATION PORT
SOURCE PIPELINE SRC
DESTINATION PIPELINE DST
130
140
TRANSFER REQUEST BUS TR BUS
117
Q0
Q1
Q2
Q3
CHANNEL REGISTERS 120

FIG. 7